WINSTAR Display

OLED SPECIFICATION

Model No:

WEH001602AGPP5N00001

OLED Specification

Contents

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WINSTAR

WINSTAR Display
華凌光電股份有限公司

Technology - Innovation - Value
Eco Friendly - Revolution

SPECIFICATION Version: 0

CUSTOMER : MODULE NO. : WEH001602AGPP5N00001

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2010/04/20		First issue

1. Module Classification Information

W E H 001602 A G P P 5 N 00001

① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

1	Brand：WINSTAR DISPLAY CORPORATION		
2	E：OLED		
3	Display Type：H→Character Type, G→Graphic Type		
4	Number of dots： 16 characters, 2Lines.		
5	Serials code		
6	Emitting Color	A：Amber	R：RED
		B：Blue	C：Full color
		G：Green	W：White
		Y：Yellow Green	L：Yellow
7	Polarizer	P：With Polarizer; N: Without Polarizer	
8	Display Mode	P：Passive Matrix ; A: Active Matrix	
9	Driver Voltage	3: 3.0 V; 5: 5.0V	
10	Touch Panel	N：Without touch panel; T: With touch panel	
11	Serial No.	00001: Sales code	

2. General Specification

Item	Dimension	Unit
Number of Characters	16 characters x 2 Lines	—
Module dimension	80.0 x 36.0 x 10.0(MAX)	mm
View area	66.0 x 16.0	mm
Active area	56.95 x 11.85	mm
Dot size	0.55 x 0.65	mm
Dot pitch	0.60x 0.70	mm
Character size	2.95 x 5.55	mm
Character pitch	3.6 x 6.3	mm
LCD type	OLED , GREEN	
Duty	1/16	

3. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Notes
Operating Temperature	T_{OP}	-40	+80	℃	
Storage Temperature	T_{ST}	-40	+80	℃	
Input Voltage	V_I	-0.3	VDD	V	
Supply Voltage For Logic	VDD-V_{SS}	-0.3	5.3	V	

4. Electrical Characteristicsical

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD-VSS	—	3.0	5.0	5.3	V
Input High Volt.	VIH	—	0.9 VDD	—	VDD	V
Input Low Volt.	VIL	—	GND	—	0.1VDD	V
Output High Volt.	VOH	IOH=-0.5mA	0.8 VDD	—	VDD	V
Output Low Volt.	VOL	IOL=0.5mA	GND	—	0.2 VDD	V
Supply Current	IDD	VDD=5V	—	30	—	mA
CIEx(GREEN)		x,y(CIE1931)	0.26	0.28	0.30	
CIEy(GREEN)		x,y(CIE1931)	0.62	0.64	0.66	

5. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ		160			deg
	(H)φ		160			deg
Contrast Ratio	CR	Dark	2000:1		—	—
Response Time	T rise	—		10		μs
	T fall	—		10		μs
Supply Voltage For Logic 5V 50% Check Board Brightness		With polarizer		125		nits
Supply Voltage For Logic 3V 50% Check Board Brightness		With polarizer		80		nits

6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground
2	VDD	5.0V	Supply Voltage for logic
3	NC	—	
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	NC	—	
16	NC	—	

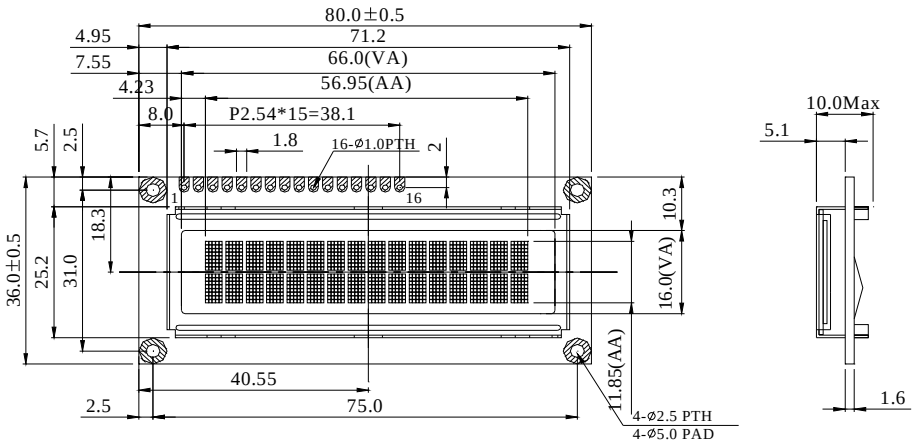
※Brightness Control

Brightness(nits)	Power consumption(measured with random texts)
125(typical)	150mW(5V*30mA)

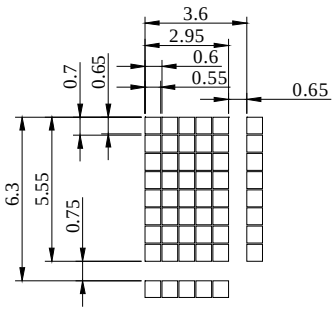
Notes: 1.When random texts pattern is running , averagely , at any instance , about 1/2 of pixels will be on.

2. You can to use the display off mode to make long life.

7. Counter Drawing & Block Diagram



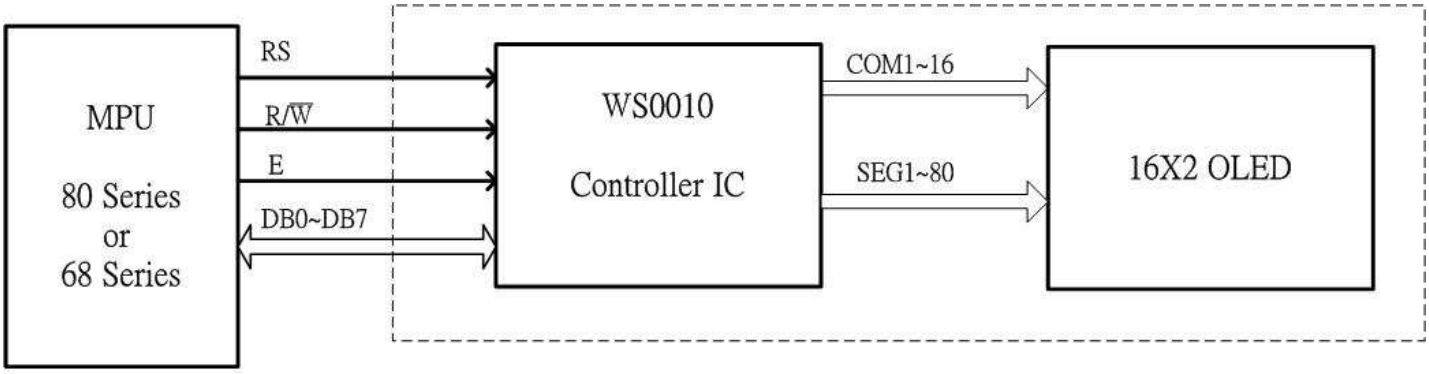
PIN NO.	SYMBOL
1	Vss
2	Vdd
3	NC
4	RS
5	R/$\overline{W}$
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	NC
16	NC



DOT SIZES

SCALE 5/1

The non-specified tolerance of dimension is ±0.3 mm .



Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CA (Character Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

1	2	3	4	.....	.....	13	14	15	16
CA10000000	CA10000001	CA10000010	CA10000011	.....	.....	CA10001100	CA10001101	CA10001110	CA10001111
CA11000000	CA11000001	CA11000010	CA11000011	.....	.....	CA11001100	CA11001101	CA11001110	CA11001111

8. Function Description

REGISTERS

IC provides two types of 8-bit registers, namely: Instruction Register (IR) and Data Register (DR). The register is selected using the RS Pin. When the RS pin is set to "0", the Instruction Register Type is selected. When RS pin is set to "1", the Data Register Type is selected. Please refer to the table below.

RS	R/WB	Operation
0	0	Instruction register write as an internal operation.
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Data register write as an internal operation (DR to DDRAM or CGRAM)
1	1	Data register read as an internal operation (DDRAM or CGRAM to DR)

INSTRUCTION REGISTER (IR)

The Instruction Register is used to store the instruction code (i.e. Display Clear, Cursor Home and others), Display Data RAM (DDRAM) Address, and the Character Generator RAM (CGRAM) Address. Instruction register can only be written from the MPU.

DATA REGISTER (DR)

The Data Register is used as a temporary storage for data that are going to be written into the DDRAM or CGRAM as well as those data that are going to be read from the DDRAM or CGRAM.

BUSY FLAG (BF)

The Busy Flag is used to determine whether IC is idle or internally operating. When IC is performing some internal operations, the Busy Flag is set to "1". Under this condition, the no other instruction will not be accepted. When RS Pin is set to "0" and R/WB Pin is set to "1", the Busy Flag will be outputted to the DB7 pin.

When IC is idle or has completed its previous internal operation, the Busy Flag is set to "0". The next instruction can now be processed or executed.

ADDRESS COUNTER (AC)

The address counter is used to assign the Display Data RAM (DDRAM) Address and the Character Generator RAM (CGRAM) Address. When Address information is written into the Instruction Register (IR), this Address information is sent from the Instruction Register to the Address Counter. At the same time, the nature of the Address (either CGRAM or DDRAM) is determined by the instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter is automatically increased or decreased by 1 (for Write or Read Function). It must be noted that when the RS pin is set to "0" and R/WB is set to "1", the contents of the Address Counter are outputted to the pins -- DB0 to DB6.

DISPLAY DATA RAM (DDRAM)

The Display Data RAM (DDRAM) is used to store the Display Data which is represented as 8-bit character code. The Display Data RAM supports an extended capacity of 128 x 8-bits or 128 characters.

The Display Data RAM Address (ADD) is set in the Address Counter as a hexadecimal.

	High Order Bits			**Low Order Bits**			
Address Counter (hex)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

An example of a DDRAM Address=39 is given below.

DDRAM Address: 39						
AC6	AC5	AC4	AC3	AC2	AC1	AC0
0	1	1	1	0	0	1

1-LINE DISPLAY (N=0)

When the number of characters displayed is less than 128, the first character is displayed at the head position. The relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position (digit)	**1**	**2**	**3**	**4**	**……**	**126**	**127**	**128**
DDRAM address (hexadecimal)	00	01	02	03	……	7D	7E	7F

For example, when only 8 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
DDRAM address	00	01	02	03	04	05	06	07
Shift left	01	02	03	04	05	06	07	08
Shift right	7F	00	01	02	03	04	05	06

2-LINE DISPLAY (N=1*)*

Case 1: The Number of Characters displayed is less than 64 x 2 lines

When the number of characters displayed is less than 64 x 2 lines, then the first character of the first and second lines are displayed starting from the head. It is important to note that every line reserve 64 x8bits DDRAM space. 1st line is 00 to 3F,second line is 40 to 7F.Please refer the figure below.

Display Position	**1**	**2**	**3**	**4**	**…….**	**61**	**62**	**63**	**64**
DDRAM Address (hexadecimal)	00	01	02	03	…….	3C	3D	3E	3F
	40	41	42	43	…….	7C	7D	7E	7F

To illustrate, for 2-line x 20 characters display, the relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position	**1**	**2**	**3**	**4**	**…….**	18	19	20
DDRAM address (hexadecimal)	00	01	02	03	**…….**	11	12	13
	40	41	42	43	**…….**	51	52	53
Shift left	01	02	03	04	**…….**	19	20	21
	41	42	43	44	**…….**	52	53	54
Shift right	3F	00	01	02	**…….**	10	11	12
	7F	40	41	42	**…….**	50	51	52

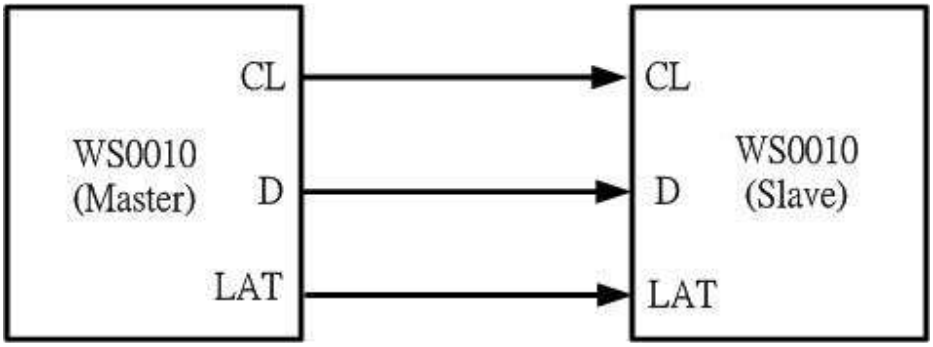
Case 2: 40-Character x 2 Lines Display
IC(Master) can be extended to display 40 characters x 2 lines by cascade the other IC(Slave). When there is a Display Shift operation, the DDRAM Address is also shifted. Please refer to the example below.

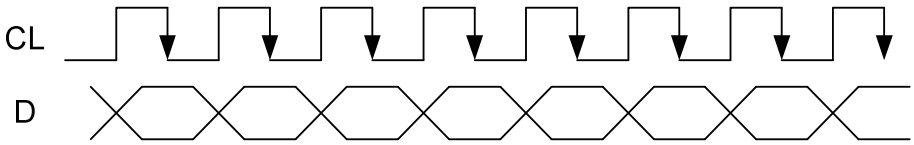
Display Position	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**….**	**37**	**38**	**39**	**40**
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	**….**	24	25	26	27
	40	41	42	43	44	45	46	47	48	49	4A	**….**	64	65	66	67
	IC display (Master)								Cascade 2nd IC(Slave)							
Shift left	01	02	03	04	05	06	07	08	09	0A	0B	**….**	25	26	27	28
	41	42	43	44	45	46	47	48	49	4A	4B	**….**	65	66	67	68
Shift right	3F	00	01	02	03	04	05	06	07	08	09	**….**	23	24	25	26
	7F	40	41	42	43	44	45	46	47	48	49	**….**	63	64	65	66

SLAVE MODE DATA INPUT

When IC is under slave mode, display data is send from the other IC(master).The input data “D” is shifted at the falling edge of CL

M/S	Mode	D	CL	LAT
H	Master	Output	Output	Output
L	Slave	Input	Input	Input

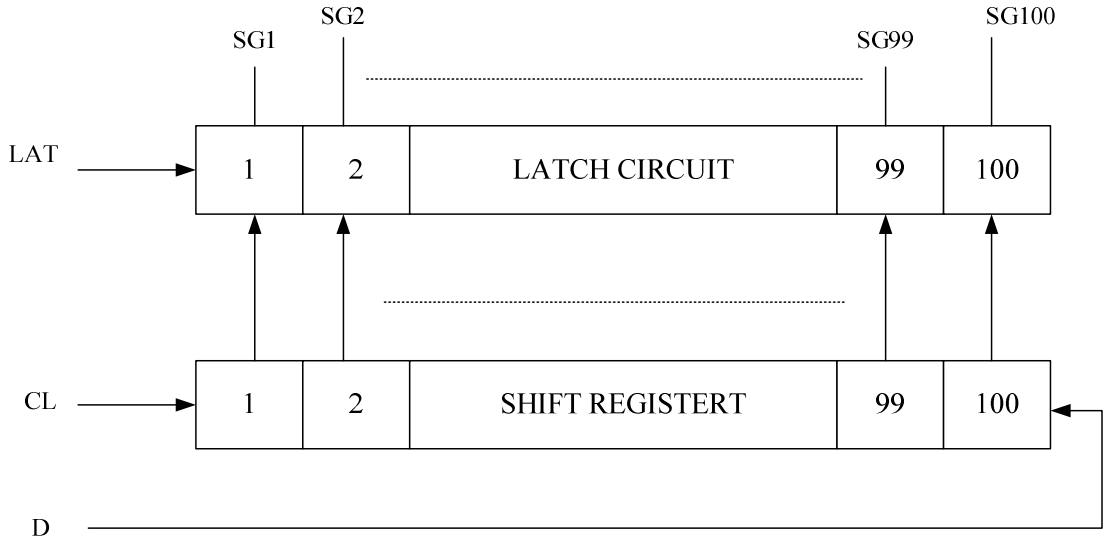




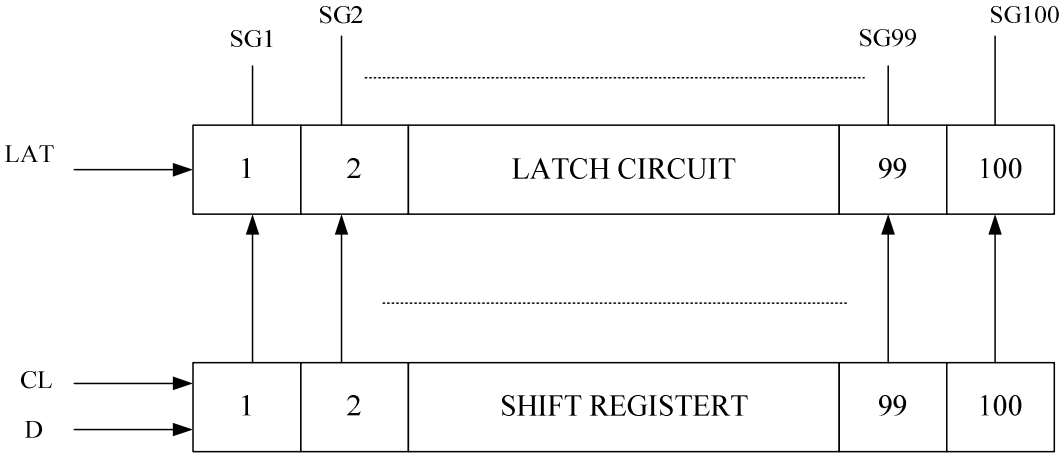
BIDIRECTIONAL SHIFT REGISTER BLOCK

This block shifts the serial data at the falling edge of CL. When SHL is set “H”, the data input from D is shifted from bit100 to bit1 (When IC is “master” mode, D is output; When IC is “slave” mode, D is input). When SHL is set “L”, the data input is shifted from bit1 to bit100.

Condition 1 : SHL=”H”



Condition 2 : SHL=”L



CHARACTER GENERATOR ROM (CGROM)

The Character Generator ROM (CGROM) is used to generate either 5 x 8 dots or 5 x 10 dots character patterns from 8-bit character codes.IC build in three set of font tables as “Western European”, ”English Japanese” and “English Russian”. User can use software to select suitable font table **(Default “English Japanese”)**.

CHARACTER GENERATOR RAM (CGRAM)

The Character Generator RAM (CGRAM) is used to generate either 5 x 8 dot or 5 x 10 dot character patterns. It can generate eight 5 x 8 dot character patterns or four 5 x 10 dot character patterns. The character patterns generated by the CGRAM can be rewritten. User-defined character patterns for the CGRAM are supported.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X 8 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									**CGRAM Address**							**Character Patterns (CGRAM Data)**								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High						Low			High				Low			High						Low		
0	0	0	0	*	0	0	0		0	0	0	0	0	0		*	*	*	1	1	1	1	0	Character pattern 1
												0	0	1		*	*	*	1	0	0	0	1	
												0	1	0		*	*	*	1	0	0	0	1	
												0	1	1		*	*	*	1	1	1	1	0	
												1	0	0		*	*	*	1	0	1	0	0	
												1	0	1		*	*	*	1	0	0	1	0	
												1	1	0		*	*	*	1	0	0	0	1	
												1	1	1		*	*	*	0	0	0	0	0	Cursor Position
0	0	0	0	*	0	0	1		0	0	1	0	0	0		*	*	*	1	0	0	0	1	Character pattern 2
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	1	1	1	1	1	
												0	1	1		*	*	*	0	0	1	0	0	
												1	0	0		*	*	*	1	1	1	1	1	
												1	0	1		*	*	*	0	0	1	0	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor position
0	0	0	0	*	. . . . .	. . . . .	. . . . .		. . .	. . .	. . .	. . .	. . .	. . .		*	*	*	. . .	. . .	. . .	. . .	. . .	Character pattern 3~7
0	0	0	0	*	1	1	1		1	1	1	0	0	0		*	*	*	0	0	0	0	0	Character pattern 8
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	0	0	0	0	0	
												0	1	1		*	*	*	0	0	0	0	0	
												1	0	0		*	*	*	1	0	0	0	1	
												1	0	1		*	*	*	0	1	1	1	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor position

Notes:
1. * = Not Relevant
2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 0 to 2 correspond to the CGRAM Address Bits 3 to 5 (3 bits: 8 types)
4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.
5. The CGRAM Address Bits 0 to 2 are used to define the character pattern line position. The 8th line is the cursor position and its display is formed by the logical OR with the cursor. The 8th line CGRAM data bits 0 to 4 must be set to "0". If any of the 8th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit 3 is not relevant and will not have any effect on the character display. Because of this, the first Character Pattern shown above (R) can be displayed when the Character Code is 00H or 08H.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X10 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address							Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High						Low			High				Low			High						Low		
0	0	0	0	*	0	0	*		0	0	0	0	0	0		*	*	*	0	0	1	0	0	Character pattern 1
											0	0	0	1		*	*	*	0	1	1	1	0	
											0	0	1	0		*	*	*	1	0	1	0	1	
											0	0	1	1		*	*	*	1	0	1	0	0	
											0	1	0	0		*	*	*	0	1	1	0	0	
											0	1	0	1		*	*	*	0	0	1	1	0	
											0	1	1	0		*	*	*	0	0	1	0	1	
											0	1	1	1		*	*	*	1	0	1	0	1	
											1	0	0	0		*	*	*	0	1	1	1	0	
											1	0	0	1		*	*	*	0	0	1	0	0	
											1	0	1	0		*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1		*	*	*	*	*	*	*	*	
											1	1	0	0		*	*	*	*	*	*	*	*	
											1	1	0	1		*	*	*	*	*	*	*	*	
											1	1	1	0		*	*	*	*	*	*	*	*	
											1	1	1	1		*	*	*	*	*	*	*	*	
0	0	0	0	*	. . .	. . .	*		. . .	. . .	. . .	. . .	. . .	. . .		*	*	*	. . .	. . .	. . .	. . .	. . .	Character pattern 2~3
0	0	0	0	*	1	1	*		1	1	0	0	0	0		*	*	*	1	0	1	0	1	Character pattern 4
											0	0	0	1		*	*	*	1	1	1	1	1	
											0	0	1	0		*	*	*	1	1	1	1	1	
											0	0	1	1		*	*	*	1	1	1	1	1	
											0	1	0	0		*	*	*	0	1	1	1	0	
											0	1	0	1		*	*	*	0	0	1	0	0	
											0	1	1	0		*	*	*	0	0	1	0	0	
											0	1	1	1		*	*	*	1	0	1	0	1	
											1	0	0	0		*	*	*	0	1	1	1	0	
											1	0	0	1		*	*	*	0	0	1	0	0	
											1	0	1	0		*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1		*	*	*	*	*	*	*	*	
											1	1	0	0		*	*	*	*	*	*	*	*	
											1	1	0	1		*	*	*	*	*	*	*	*	
											1	1	1	0		*	*	*	*	*	*	*	*	
											1	1	1	1		*	*	*	*	*	*	*	*	

Notes:
1. * = Not Relevant
2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 1 and 2 correspond to the CGRAM Address Bits -- 4 and 5 respectively (2 bits : 4 types)
4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.
5. The CGRAM Address Bits 0 to 3 are used to define the character pattern line position. The 11th line is the cursor position and its display is formed by the logical OR with the cursor. The 11th line CGRAM data bits 0 to 4 must be set to "0". If any of the 11th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit -- 0 and 3 are not relevant and will not have any effect on the character display. Because of this, the Character Pattern shown above ($) can be displayed when the Character Code is 00H, 01H, 08H or 09H.

TIMING GENERATION CIRCUIT

The timing signals for the internal circuit operations (i.e. DDRAM, CGRAM, and CGROM) are generated by the Timing Generation Circuit. The timing signals for the MPU internal operation and the RAM Read for Display are generated separately in order to prevent one from interfering with the other. This means that, for example, when the data is being written into the DDRAM, there will be no unwanted interference such as flickering in areas other than the display area.

OLED DRIVER CIRCUIT

IC provides 16 Common Drivers and 100 Segment Driver Outputs. When a character font and the number of lines to be displayed have been selected, the corresponding Common Drivers output the waveform automatically. A non-selection waveform will be outputted by the rest of the Common outputs.

CURSOR/BLINK CONTROL CIRCUIT

The cursor or character blinking is generated by the Cursor / Blink Control Circuit. The cursor or the blinking will appear with the digit located at the Display Data RAM (DDRAM) Address Set in the Address Counter (AC).

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Address counter	0	0	0	0	1	1	1

CASE 1: FOR 1-LINE DISPLAY

Example: When the Address Counter (AC) is set to 0EH, the cursor position is displayed at DDRAM Address 0EH.

Display position	1	2	3	4	5	……	14	15	……	19	20
DDRAM address (hexadecimal)	00	01	02	03	04	……	0D	**0E**	……	12	13

Cursor Position

Notes:
The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in a irrelevant and meaningless position.

CASE 2: FOR 2-LINE DISPLAY

Example: When the Address Counter (AC) is set to 46H, the cursor position is displayed at DDRAM Address 46H.

Display position	1	2	3	4	5	6	7	8	……	19	20
DDRAM address	00	01	02	03	04	05	06	07	……	09	13
(hexadecimal)	40	41	42	43	44	45	46	47	……	49	53

Cursor Position
Notes:
The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in an irrelevant and meaningless position.

CHARACTER MODE ADDRESSING

WIN0010 provides two kind of character mode. User can fill in 128 characters data (N=0, one line) or 64 characters data per line (N=1, two line) in embedded RAM to display graphic. Character mode address can be controlled by DDRAM address instruction.

Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CA (Character Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

(1)1-Line condition (N=0)

1	2	3	4	……	……	125	126	127	128
CA=10000000	CA=10000001	CA=10000010	CA=10000011			CA=11111100	CA=11111101	CA=11111110	CA=11111111

(2)2-Line condition (N=1)

1	2	3	4	……	……	61	62	63	64
CA=10000000	CA=10000001	CA=10000010	CA=10000011			CA=10111100	CA=10111101	CA=10111110	CA=10111111
CA=11000000	CA=11000001	CA=11000010	CA=11000011			CA=11111100	CA=11111101	CA=11111110	CA=11111111

GRAPHIC MODE ADDRESSING

WIN0010 provides not only character mode but also graphic mode. User can fill in 100x16 data in embedded RAM to display graphic. Graphic mode addressing is different from character mode.

Use DDRAM address instruction to set X-axis address of Graphic mode and CGRAM address instruction to set Y-axis of Graphic mode.

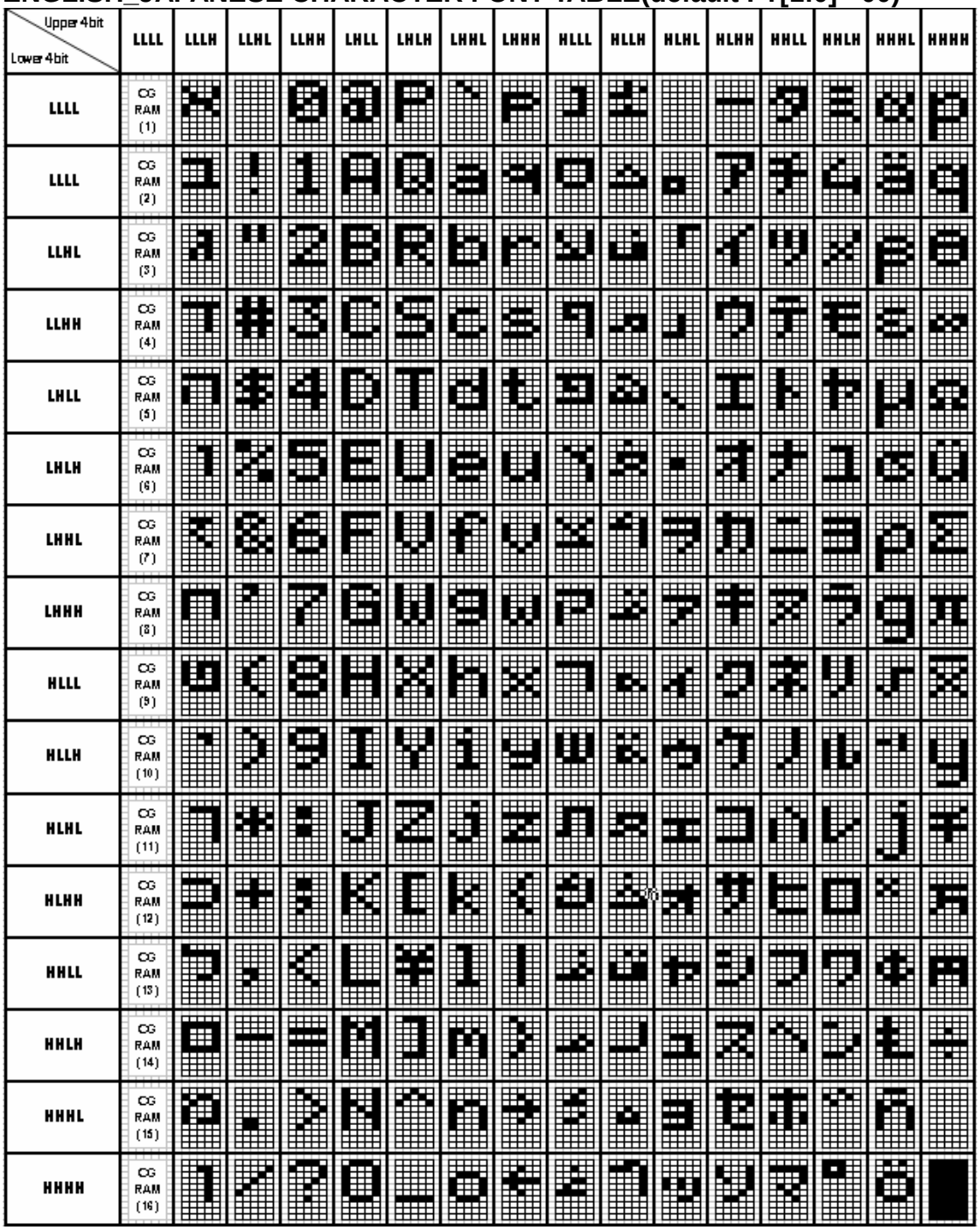
Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GXA (Graphic X-axis Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
GYA (Graphic Y-axis Address)	0	1	0	0	0	0	0	CGA0

	1	2	3	4	……	……	97	98	99	100
CGA0=0	GXA=10000000 GYA=01000000	GXA=10000001 GYA=01000000	GXA=10000010 GYA=01000000	GXA=10000011 GYA=01000000	D0 D1 D2 D3 D4 D5 D6 D7		GXA=11100000 GYA=01000000	GXA=11100001 GYA=01000000	GXA=11100010 GYA=01000000	GXA=11100011 GYA=01000000
CGA0=1	GXA=10000000 GYA=01000001	GXA=10000001 GYA=01000001	GXA=10000010 GYA=01000001	GXA=10000011 GYA=01000001	D0 D1 D2 D3 D4 D5 D6 D7		GXA=11100000 GYA=01000001	GXA=11100001 GYA=01000001	GXA=11100010 GYA=01000001	GXA=11100011 GYA=01000001

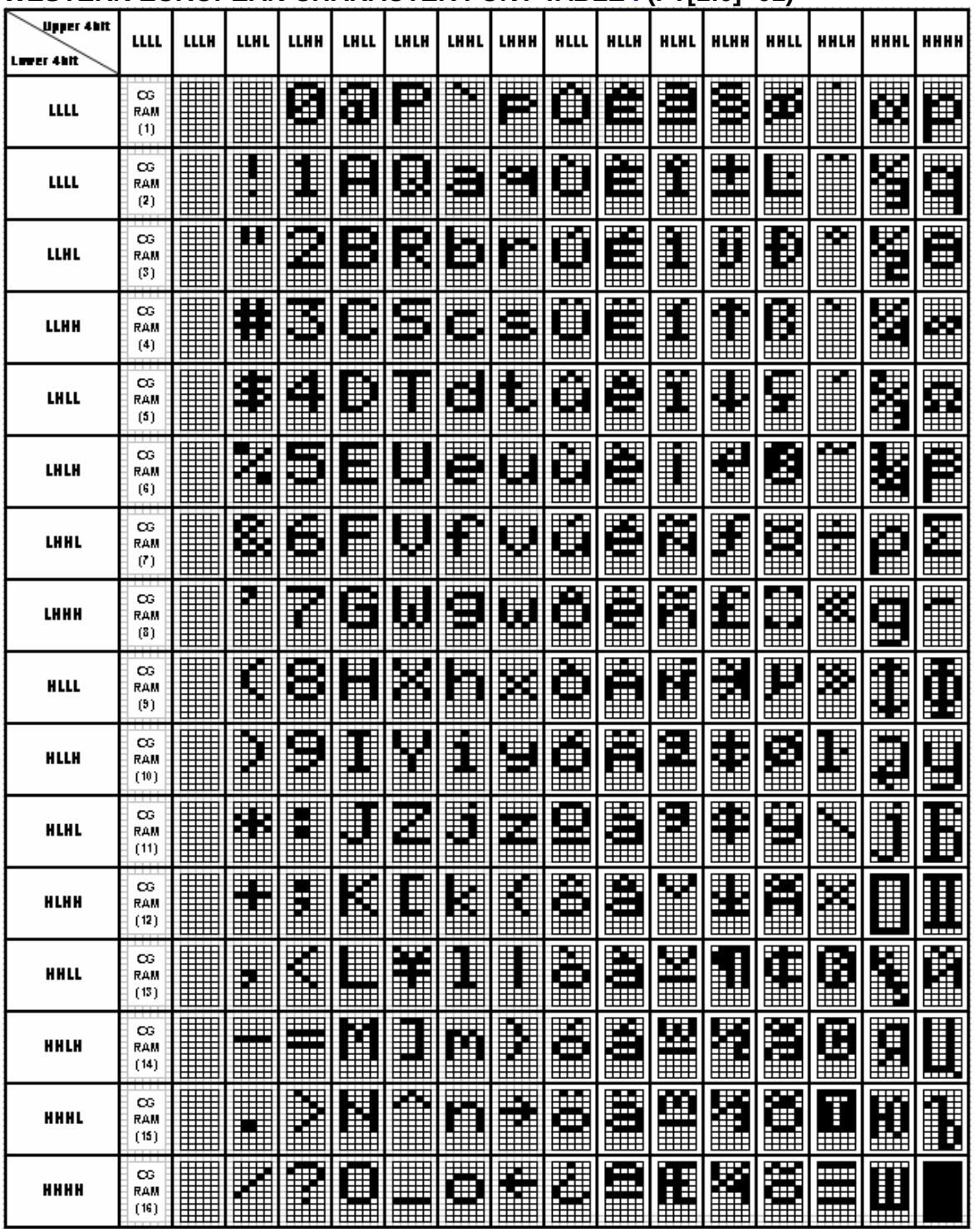
9.Character Generator ROM Pattern

CHARACTER GENERATOR ROM (CGROM)
WIN0010 provides three set of character font. Character font can be selected by programming FT.

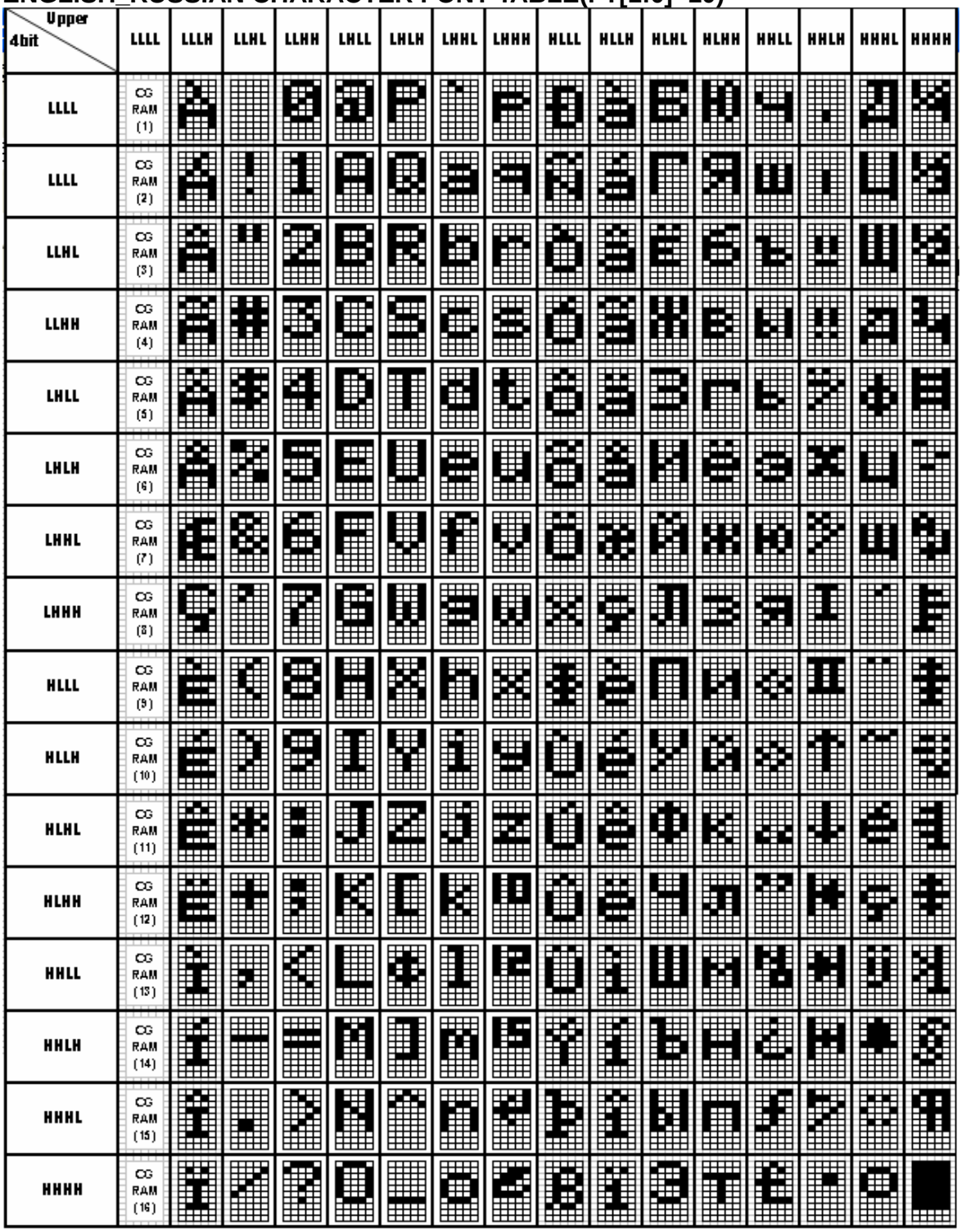
ENGLISH_JAPANESE CHARACTER FONT TABLE(default FT[1:0]= 00)



WESTERN EUROPEAN CHARACTER FONT TABLE I (FT[1:0]=01)



ENGLISH_RUSSIAN CHARACTER FONT TABLE(FT[1:0]=10)



WESTERN EUROPEAN CHARACTER FONT TABLE II (FT[1:0]=1

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLL	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (9)															
HLLH	CG RAM (10)															
HLHL	CG RAM (11)															
HLHH	CG RAM (12)															
HHLL	CG RAM (13)															
HHLH	CG RAM (14)															
HHHL	CG RAM (15)															
HHHH	CG RAM (16)															

10. Instruction Table

Instruction	Code										Description	Max. Execution Time when fsp or fosc = 250KHz
	RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display. Sets DDRAM Address 0 into the Address Counter	6.2ms
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM Address 0 into the Address Counter. Returns shifted display to original position. DDRAM contents remain unchanged. (DB0 is test pin. User should set DB0=0 all the time)	0
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. (These operations are performed during data write and read.)	0
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets entire Display (D) ON/OFF. Sets Cursor (C) ON/OFF. Sets Blinking (B) of Cursor Position Character.	0
Cursor/ Display Shift/ Mode/ Pwr	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor & shifts display without changing DDRAM contents.	0
							G/C	PWR	1	1	Sets Graphic/Character Mode Sets internal power on/off	
Function Set	0	0	0	0	1	DL	N	F	FT1	FT0	Sets interface data length (DL). Sets number of display lines (N). Sets Character Font (F). Sets Font Table (FT)	0
et CGRAM Address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM Address. CGRAM data is sent and received after this setting.	0
et DDRAM Address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM Address. The DDRAM data Is sent and received after this setting.	0
ead Busy Flag & Address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads Busy Flag (BF) indicating that internal operation is being performed. Reads Address Counter contents.	0
Write data into the CGRAM or DDRAM	1	0	Write Data								Writes data into the CGRAM or DDRAM	0
Read Data from the CGRAM or DDRAM	1	1	Read Data								Read data from the CGRAM or DDRAM	0

11. Timing Characteristics

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

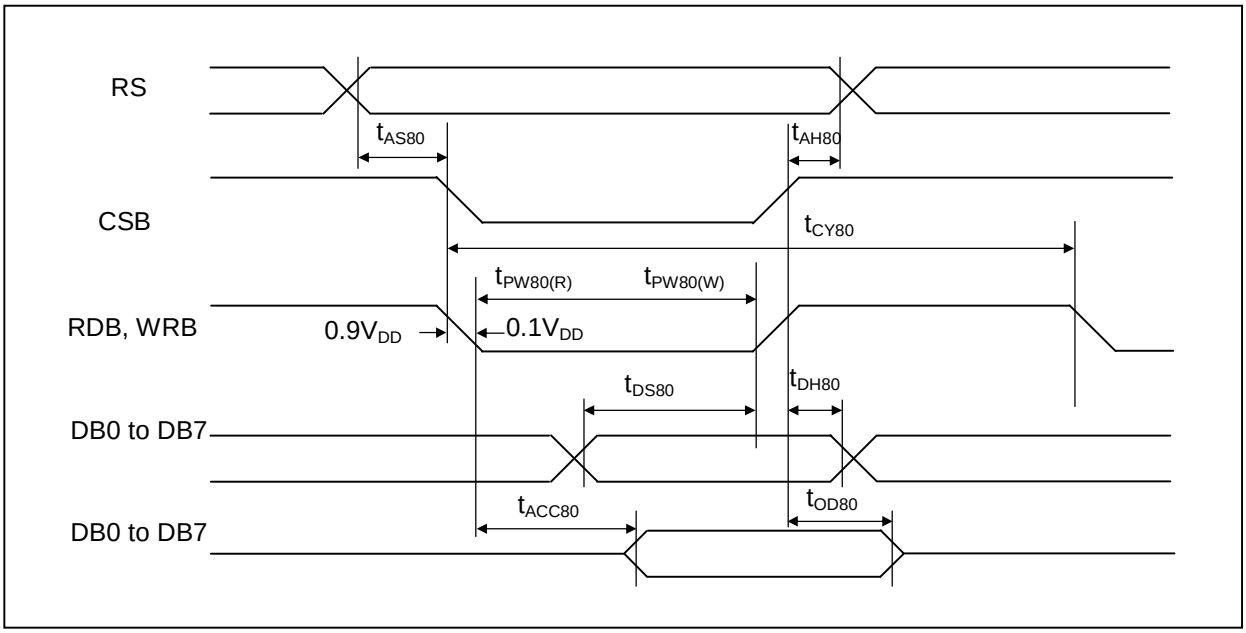


Figure 1. Read / Write Characteristics (8080-series MPU)

VDD = 3.0 to 5.3V, Ta = 25℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t**AS80** t**AH80**	20 0	-	-	ns	
System cycle time		t**CY80**	500	-	-	ns	
Pulse width (WRB)	RW_WRB	t**PW80**(W)	250	-	-	ns	
Pulse width (RDB)	E_RDB	t**PW80**(R)	250	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t**DS80** t**DH80**	40 20	-	-	ns	
Read access time Output disable time		t**ACC80** t**OD80**	- 10	-	180 -	ns	C**L** = 100pF

Read / Write Characteristics (6800-series Microprocessor)

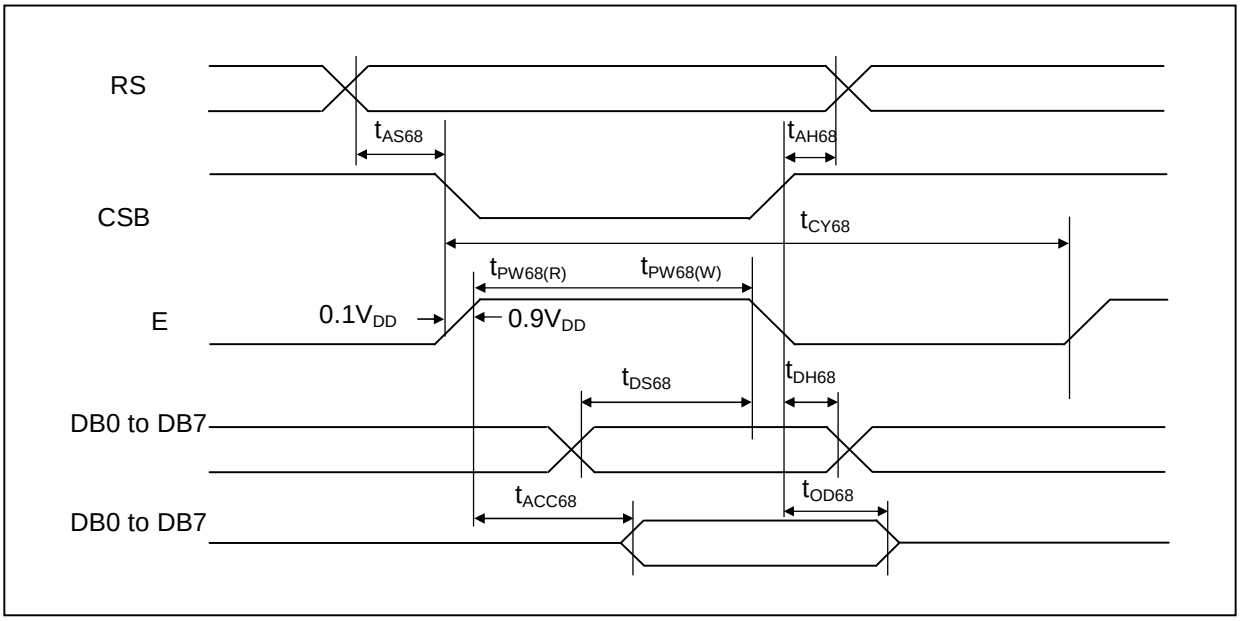


Figure 2. Read / Write Characteristics (6800-series MPU)

(VDD = 3.0 to 5.3V, Ta = 25℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t**AS68** t**AH68**	20 0	-	-	ns	
System cycle time		t**CY68**	500	-	-	ns	
Pulse width (E)	E_RDB	t**PW68**(W)	250	-	-	ns	
Pulse width (E)	E_RDB	t**PW68**(R)	250	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t**DS68** t**DH68**	40 20	-	-	ns	
Read access time Output disable time		t**ACC68** t**OD68**	- 10	-	180 -	ns	CL = 100pF

Serial Interface Characteristics

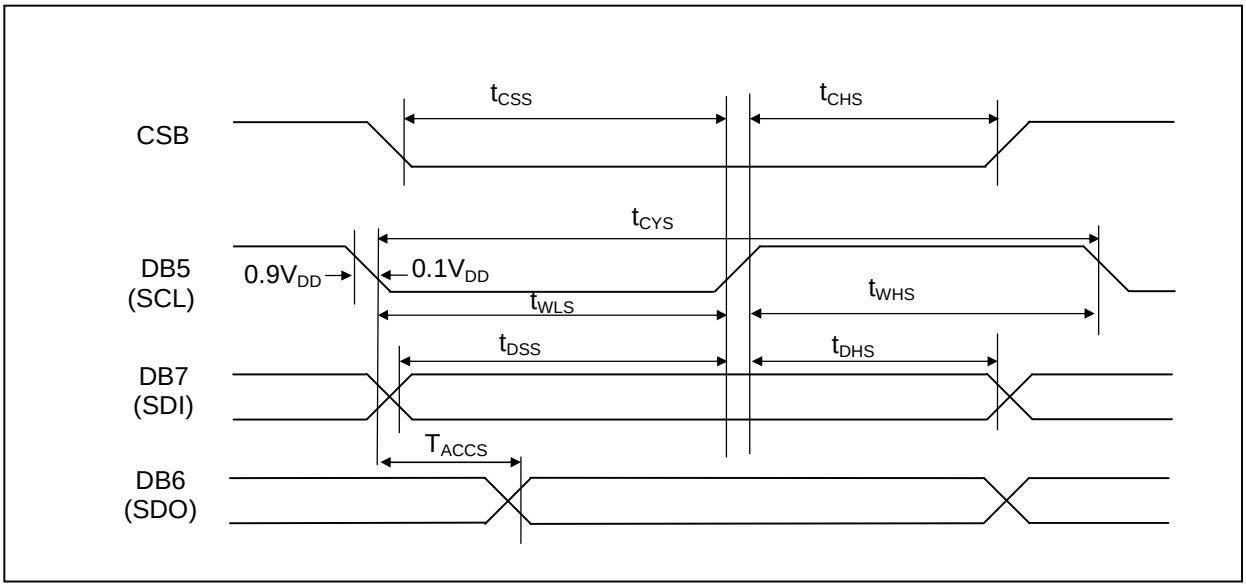


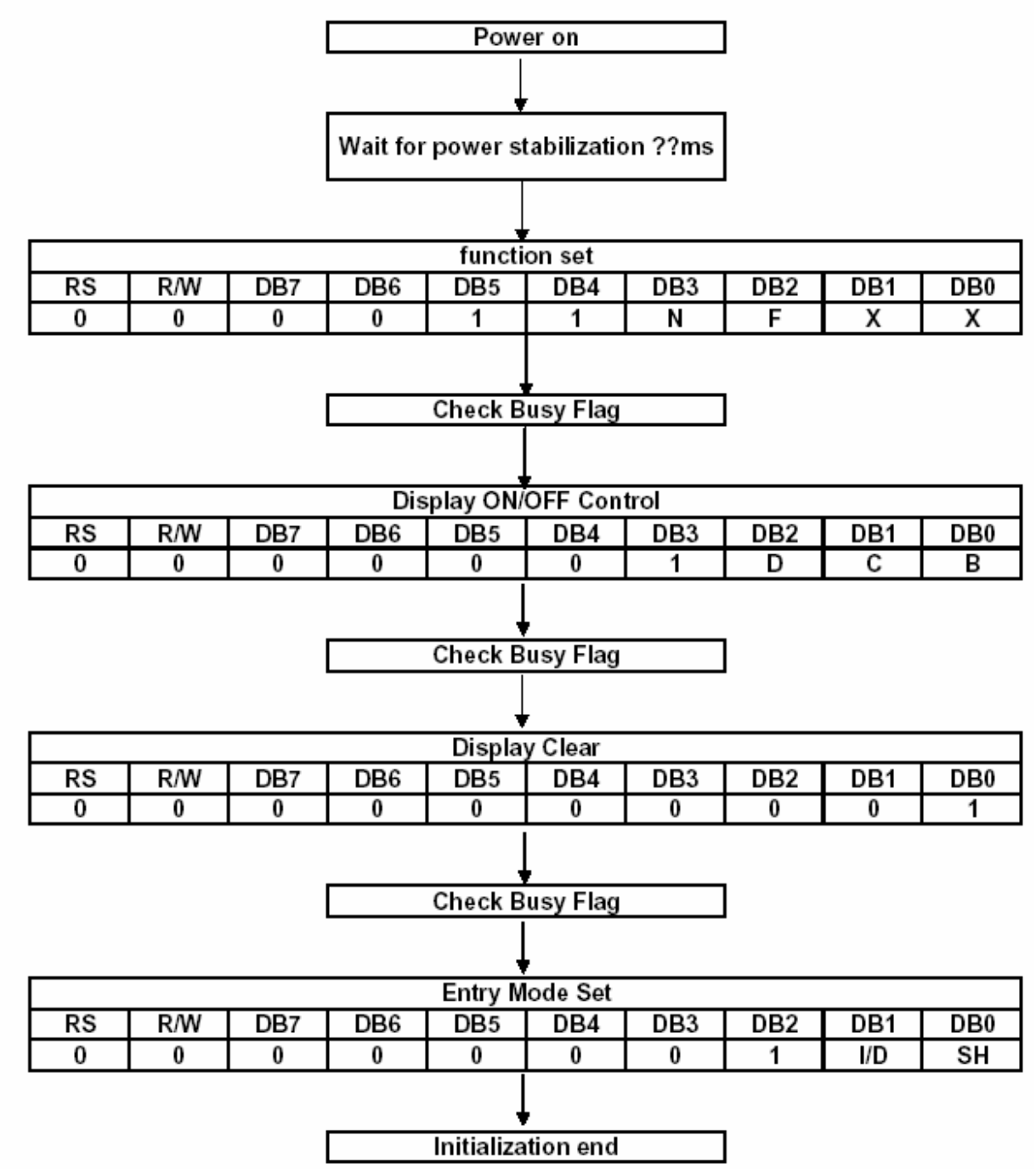
Figure 3. Serial Interface Characteristics

(VDD = 3.0 to 5.3V, Ta = 25℃)

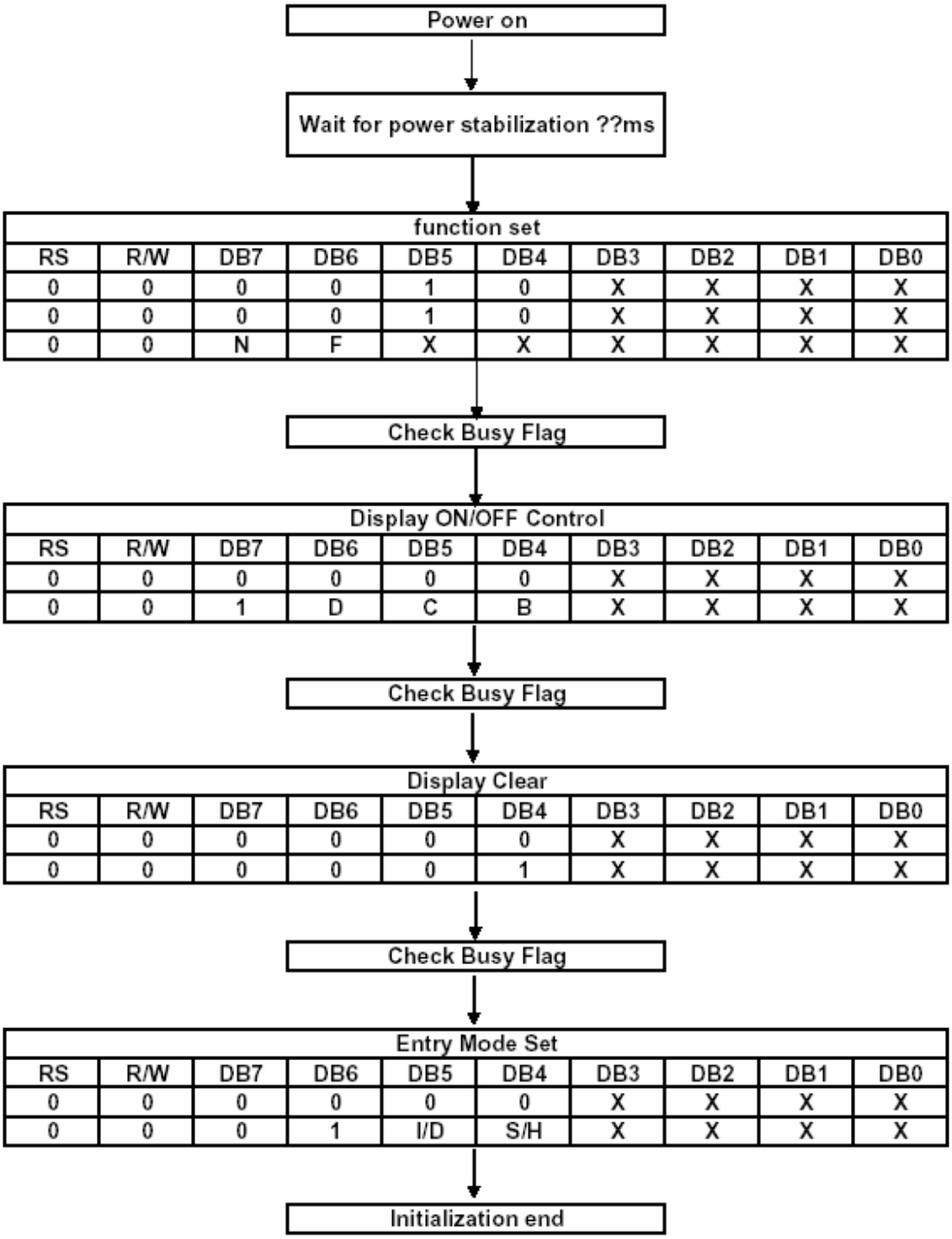
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB5 (SCL)	t**CYS** t**WHS** t**WLS**	300 100 100	- - -	- - -	ns	
CSB setup time CSB hold time	CSB	t**CSS** t**CHS**	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	t**DSS** t**DHS**	100 100	- -	- -	ns	
Read access time	DB6 (SDO)	t**ACC**S	-	-	80	ns	

12. Initializing of OLED Module

(1)8-bit mode



(2)4-bit mode


Power on
Wait for power stabilization ??ms
function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 0 X X X X
0 0 0 0 1 0 X X X X
0 0 N F X X X X X X
Check Busy Flag
Display ON/OFF Control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 1 D C B X X X X
Check Busy Flag
Display Clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 0 0 0 1 X X X X
Check Busy Flag
Entry Mode Set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 0 1 I/D S/H X X X X
Initialization end

INSTRUCTIONS

WIN0010's Instruction Register (IR) and Data Register (DR) are the only registers that can be controlled by the MPU. Prior to the commencement of it internal operation, WIN0010 temporarily stores the control information to its Instruction Register (IR) and Data Register (DR) in order to easily facilitate interface with various types of MPU. The internal operations of the WIN0010 are determined by the signals (RS, R/WB, DB0 to DB7) that are sent from the MPU. These signals are categorized into 4 instructions types, namely:

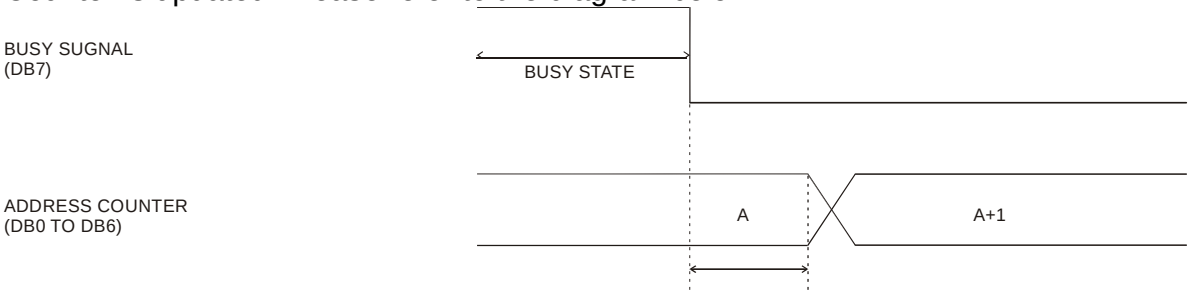
1, Function Setting Instructions (i.e. Display, Format, Data Length etc.)
2. Internal RAM Address Setting Instructions
3. Data Transfer with Internal RAM Instructions
4. Miscellaneous Function Instructions

The generally used instructions are those that execute data transfers with the internal RAM. However, when the internal RAM addresses are auto incremented/decremented by 1 after each Data Write, the program load of the MPU is lightened. The Display Shift Instruction can be executed at the same time as the Display Data Write, thereby minimizing system development time with maximum programming efficiency.

When an instruction is being executed for an internal operation, only the Busy Flag/Address Read Instruction can be performed. The other instructions are not valid. It should be noted that during the execution of an instruction, the Busy Flag is set to "1". The Busy Flag is set to "0" when the instructions are can be accepted and executed. Therefore, the Busy Flag should be checked to make certain that BF = "0" before sending another instruction from the MPU. If not, the time between the first instruction and the next instruction is longer than the time it takes to execute the instruction itself.

Instruction	Code										Description	Max. Execution Time when fsp or fosc = 250KHz
	RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display. Sets DDRAM Address 0 into the Address Counter	6.2ms
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM Address 0 into the Address Counter. Returns shifted display to original position. DDRAM contents remain unchanged. (DB0 is test pin. User should set DB0=0 all the time)	0
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. (These operations are performed during data write and read.)	0
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets entire Display (D) ON/OFF. Sets Cursor (C) ON/OFF. Sets Blinking (B) of Cursor Position Character.	0
Cursor/ Display Shift/ Mode/ Pwr	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor & shifts display without changing DDRAM contents.	0
							G/C	PWR	1	1	Sets Graphic/Character Mode Sets internal power on/off	
Function Set	0	0	0	0	1	DL	N	F	FT1	FT0	Sets interface data length (DL). Sets number of display lines (N). Sets Character Font (F). Sets Font Table (FT)	0
et CGRAM Address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM Address. CGRAM data is sent and received after this setting.	0
et DDRAM Address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM Address. The DDRAM data Is sent and received after this setting.	0
ead Busy Flag & Address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads Busy Flag (BF) indicating that internal operation is being performed. Reads Address Counter contents.	0
Write data into the CGRAM or DDRAM	1	0	Write Data								Writes data into the CGRAM or DDRAM	0
Read Data from the CGRAM or DDRAM	1	1	Read Data								Read data from the CGRAM or DDRAM	0

Notes:
1. After the CGRAM/DDRAM Read or Write Instruction has been executed, the RAM Address Counter is incremented or decremented by 1. After the Busy Flag is turned OFF, the RAM Address is updated.
2. I/D=Increment/Decrement Bit
- I/D="1": Increment
- I/D="0": Decrement
3. S=Shift Entire Display Control Bit. When S=”0”, shift function disable.
4. BF=Busy Flag
- BF="1": Internal Operating in Progress
- BF="0": No Internal Operation is being executed, next instruction can be accepted.
5. R/L=Shift Right/Left
- R/L="1": Shift to the Right
- R/L="0": Shift to the Left
6. S/C=Display Shift/Cursor Move
- S/C="1": Display Shift
- S/C="0": Cursor Move
7. G/C=Graphic/Character mode selection. G/C=”0”, Character mode is selected. G/C=”1”, Graphic mode is selected.
8. PWR=Internal DCDC on/of control. PWR=”1”, DCDC on. PWR=”0”, DCDC off.
9. DDRAM=Display Data RAM
10. CGRAM=Character Generator RAM
11. ACG=CGRAM Address
12. ADD=Address Counter Address (corresponds to cursor address)
13. AC=Address Counter (used for DDRAM and CGRAM Addresses)
14. F=Character Pattern Mode
- F="1": 5 x 10 dots
- F="0": 5 x 8 dots
15. N=Number of Lines Displayed
- N="1": 2 -Line Display
- N="0": 1-Line Display
16. tADD is the time period starting when the Busy Flag is turned OFF up to the time the Address Counter is updated. Please refer to the diagram below.



INSTRUCTION DESCRIPTION

CLEAR DISPLAY INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction is used to clear the Display Write Space 20H in all DDRAM Addresses. That is, the character pattern for the Character Code 20H must be a BLANK pattern. It then sets the DDRAM Address 0 into the Address Counter and reverts the display to its original state (if the display has been shifted). The display will be cleared and the cursor or blinking will go to the left edge of the display. If there are 2 lines displayed, the cursor or blinking will go to the first line 's left edge of the display.
Under the Entry Mode, this instruction also sets the I/D to 1 (Increment Mode). The S Bit of the Entry Mode does not change.

RETURN HOME INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Note: * = Not Relevant

This instruction is used to set the DDRAM Address 0 into the Address Counter and revert the display to its original status (if the display has been shifted). The DDRAM contents do not change.
The cursor or blinking will go to the left edge of the display. If there are 2 lines displayed, the cursor or blinking will go to the first line's left edge of the display.

ENTRY MODE SET INSTRUCTION

The Entry Mode Set Instruction has two controlling bits: I/D and S. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

I/D IS THE INCREMENT/DECREMENT BIT.

When I/D is set to "1", the DDRAM Address is incremented by "1" when a character code is written into or read from the DDRAM. An increment of 1 will move the cursor or blinking one step to the right.

When I/D is set to "0", the DDRAM is decremented by 1 when a character code is written into or read from the DDRAM. A decrement of 1 will move the cursor or blinking one step to the left.

S: SHIFT ENTIRE DISPLAY CONTROL BIT

This bit is used to shift the entire display. When S is set to "1", the entire display is shifted to the right (when I/D ="0") or left (when I/D ="1"). When S is set to "0", the display is not shifted.

Ex1 : I/D=1, S=1

		1	2	3	4	_	Initial display
	1	2	3	4	A	_	Input new character "A"
1	2	3	4	A	B	_	Input new character "B"
2	3	4	A	B	C	_	Input new character "C"
3	4	A	B	C	D	_	Input new character "D"

Ex2 : I/D=0, S=1

1	2	3	4	_			Initial display
	1	2	3	4	A		Input new character "A"
		1	2	3	B	A	Input new character "B"
			1	2	C	B	Input new character "C"
				1	D	C	Input new character "D"

DISPLAY ON/OFF CONTROL INSTRUCTION

The Display On / OFF Instruction is used to turn the display ON or OFF. The controlling bits are D, C and B.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D: DISPLAY ON/OFF BIT

When D is set to "1", the display is turned ON. When D is set to "0", the display is turned OFF and the display data is stored in the DDRAM. The display data can be instantly displayed by setting D to "1".

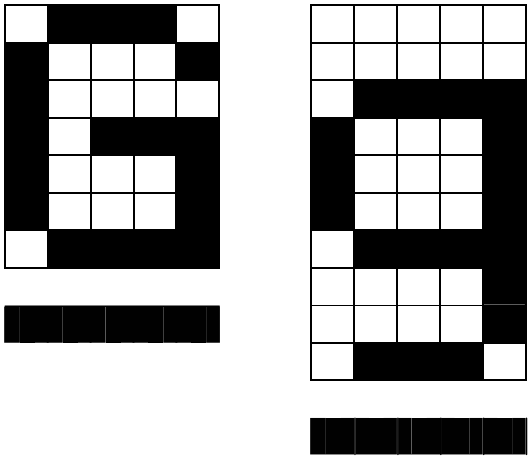
C: CURSOR DISPLAY CONTROL BIT

When C is set to "1", the cursor is displayed. In a 5 x 8 dot character font, the cursor is displayed via the 5 dots in the 8th line. In a 5 x 10 dot character font, it is displayed via 5 dots in the 11th line.

When C is set to "0", the cursor display is disabled.
During a Display Data Write, the function of the I/D and others will not be altered even if the cursor is not present. Please refer to the figure below.

5 x 8 Dot Character Font

5 x 10 Dot Character Font



Cursor

Cursor

B: BLINKING CONTROL BIT

When B is set to '1", the character specified by the cursor blinks. The blinking feature is displayed by switching between the blank dots and the displayed character at a speed of 409.6ms intervals when the fcp or fosc is 250kHz. Please refer to the figure below.

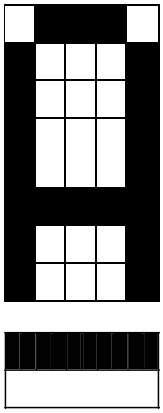


Figure 1

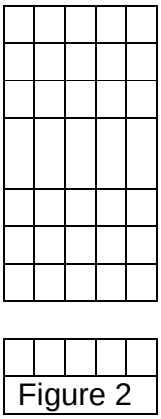


Figure 2

Note: Figures 1 and 2 are alternately displayed
The cursor and the blinking can be set to display at the same time. The blinking frequency depends on the fosc or the reciprocal of fcp.
To illustrate, when fosc=TBD Hz, then, the blinking frequency=409.6 x 250/270=379.2ms

CURSOR/DISPLAY SHIFT INSTRUCTION

This instruction is used to shift the cursor or display position to the left or right without writing or reading the Display Data. This function is used to correct or search the display. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	0	0
0	0	0	0	0	1	G/C	PW	1	1

S/C	R/L	Shift Function
0	0	Shifts the cursor position to the left. (AC is decremented by 1).
0	1	Shifts cursor position to the right. (AC incremented by 1).
1	0	Shifts entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

In a 2-line Display, the cursor moves to the second line when it passes the 40th digit of the first line. The first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly, each line moves only horizontally. The second line display does not shift into the first line position.

The Address Counter (AC) contents will not change if the only action performed is a Display Shift.

G/C: GRAPHIC MODE / CHARACTER MODE SELECTION

This bit is used to select the display mode for further process.
When G/C = 1, the *GRAPHIC MODE* will be selected.
When G/C = 0, the *CHARACTER MODE* will be selected.

PWR: ENABLE/DISABLE INTERNAL POWER

This bit is used to turn ON or turn OFF the internal power.
When PWR = 1, the internal power is turned ON.
When PWR = 0, the internal power is turned OFF.

FUNCTION SET INSTRUCTION

The Function Set Instruction has three controlling 3 bits, namely: DL, N and F. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	FT1	FT0

DL: INTERFACE DATA LENGTH CONTROL BIT

This is used to set the interface data length. When DL is set to "1", the data is sent or received in 8-bit length via the DB0 to DB7 (for an 8-Bit Data Transfer). When DL is set to "0", the data is sent or received in 4-bit length via DB4 to DB7 (for a 4-Bit Data Transfer). When the 4-bit data length is selected, the data must be sent or received twice.

N: NUMBER OF DISPLAY LINE

This is used to set the number of display lines. When N="1", the 2-line display is selected. When N is set to "0", the 1-line display is selected.

F: CHARACTER FONT SET

This is used to set the character font set. When F is set to "0", the 5 x 8 dot character font is selected. When F is set to "1", the 5 x 10 dot character font is selected.

It must be noted that the character font setting must be performed at the head of the program before executing any instructions other than the Busy Flag and Address Instruction. Otherwise, the Function Set Instruction cannot be executed unless the interface data length is changed.

FT1, FT0: FONT TABLE SELECTION

These two bits are used to select one font table out of the three for further process.
When (FT1, FT0) = (0, 0), the *ENGLISH_JAPANESE CHARACTER FONT TABLE* will be selected.
(FT1, FT0) = (0, 1), the *WESTERN EUROPEAN CHARACTER FONT TABLE* will be selected.
(FT1, FT0) = (1, 0), the *ENGLISH_RUSSIAN CHARACTER FONT TABLE* will be selected.
(FT1, FT0) = (1, 1), N/A
Note: The default setting for FT1 and FT0 is 0 and 0 respectively which means the default Font Table is *ENGLISH_JAPANESE CHARACTER FONT TABLE.*

SET CGRAM ADDRESS INSTRUCTION

This instruction is used to set the CGRAM Address binary AAAAAA into the Address Counter. Data is then written to or read from the MPU for CGRAM.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	ACG	ACG	ACG	ACG	ACG	ACG

Note: ACG is the CGRAM Addres

SET DDRAM ADDRESS INSTRUCTION

This instruction is used to set the DDRAM Address binary AAAAAAA into the Address Counter. The data is written to or read from the MPU for the DDRAM. If 1-line display is selected (N="0"), then AAAAAAA can be 00H to 4FH. When the 2-line display is selected, then AAAAAAA can be 00H to 27H for the first line and 40H to 67H for the second line.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD

Note: ADD = DDRAM Address

READ BUSY FLAG AND ADDRESS INSTRUCTION

This instruction is used to read the Busy Flag (BF) to indicate if WIN0010 is internally operating on a previously received instruction. If BF is set to "1", then the internal operation is in progress and the next instruction will not be accepted. If the BF is set to "0", then the previously received instruction has been executed and the next instruction can be accepted and processed. It is important to check the BF status before proceeding to the next write operation. The value of the Address Counter in binary AAAAAAA is simultaneously read out. This Address Counter is used by both the CGRAM and the DDRAM and its value is determined by the previous instruction. The contents of the address are the same as for the instructions -- Set CGRAM Address and Set DDRAM Address.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC	AC	AC	AC	AC	AC	AC

Notes:
1. BF=Busy Flag
2. AC=Address Counter

WRITE DATA TO **CGRAM / DDRAM INSTRUCTION**

This instruction writes 8-bit binary data -- DDDDDDDD to the CGRAM or the DDRAM. The previous CGRAM or DDRAM Address setting determines whether a data is to be written into the CGRAM or the DDRAM. After the write process is completed, the address is automatically incremented or decremented by 1 in accordance with the Entry Mode instruction. It must be noted that the Entry Mode instruction also determines the Display Shift.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D	D	D	D	D	D	D	D

READ DATA FROM THE CGRAM OR DDRAM INSTRUCTION

This instruction reads the 8-bit binary data -- DDDDDDDD from the CGRAM or the DDRAM. The Set CGRAM Address or Set DDRAM Address Set Instruction must be executed before this instruction can be performed, otherwise, the first Read Data will not be valid.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D	D	D	D	D	D	D	D

MPU INTERFACE

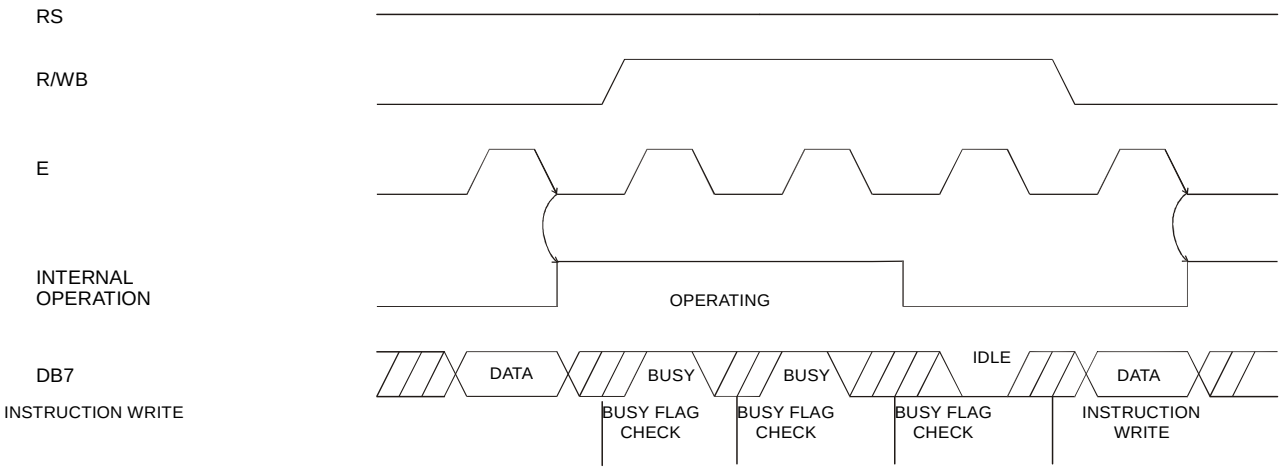
WIN0010 provides High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series and serial interface. User can choice by signal “PS” and “C68”.

68 – series interface

(a) 8-BIT mode(Not available for serial mode)

When WIN0010 interfaces with an 8-bit MPU, DB0 to DB7 are used. The 8-bit data transfer starts from the four high order bits --DB4 to DB7 followed by the four low order bits -- DB0 to DB3.

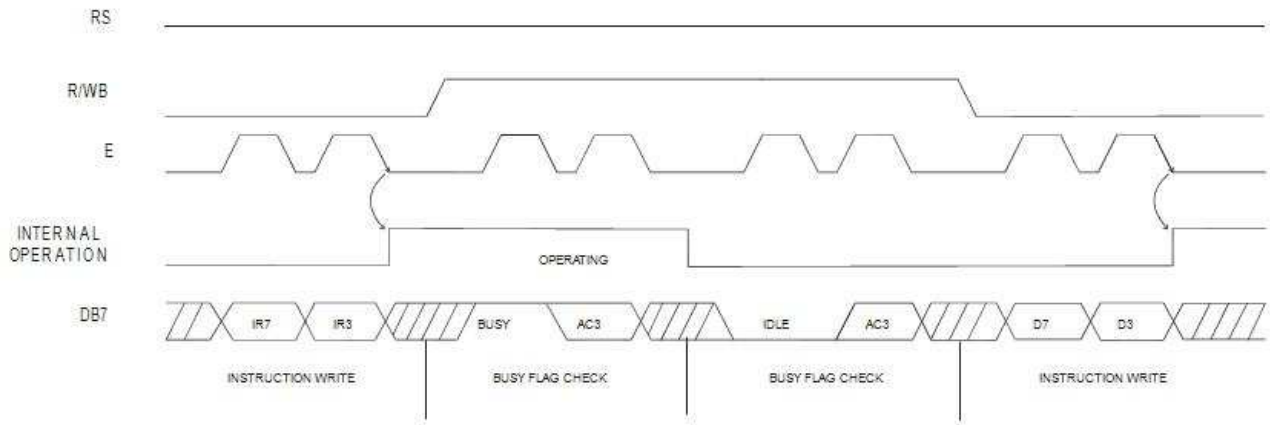
An example of a Busy Flag Check Timing in an 8-Bit MPU Interface is given in the diagram below.



(b) 4-BIT mode (Not available for serial mode)

WIN0010 can be configured to interface with a 4-bit MPU and is selected via a program. If the I/O port of the 4-Bit MPU from which WIN0010 is connected to, is capable of transferring 8 bits, then an 8-bit data transfer operation is executed. Otherwise, two 4-bit data transfer operations are needed to satisfy one complete data transfer.

Under the 4-bit data transfer, DB4 to DB7 are used as bus lines. DB0 to DB3 are disabled. The data transfer between WIN0010 and MPU is completed after two 4-bit data have been transferred. The Busy Flag must be checked (one instruction) after completion of the data transfer (that is, 4-bit data has been transferred twice.). The Busy Flag must be checked after two 4-bits data transfer has been completed. Please refer to the diagram below for a 4-bit data transfer timing sequence.

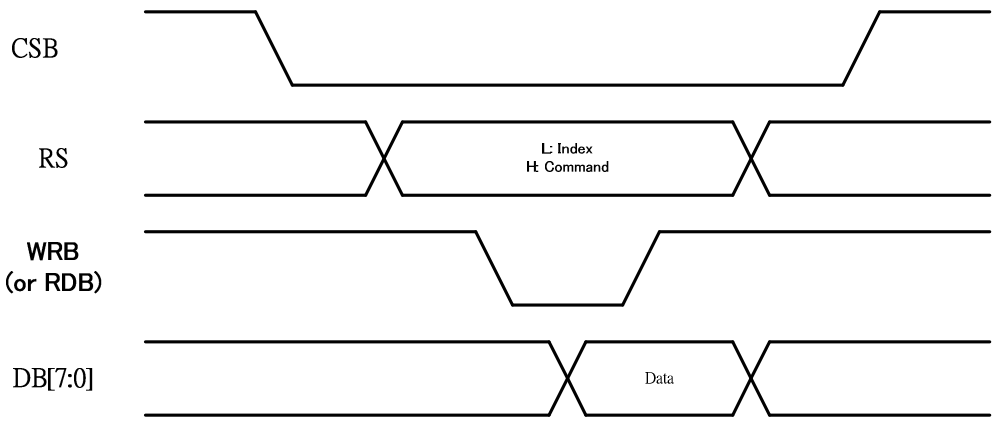


where:
1. IR7=Instruction Bit 7
2. IR3=Instruction Bit 3
3. AC3=Address Counter 3

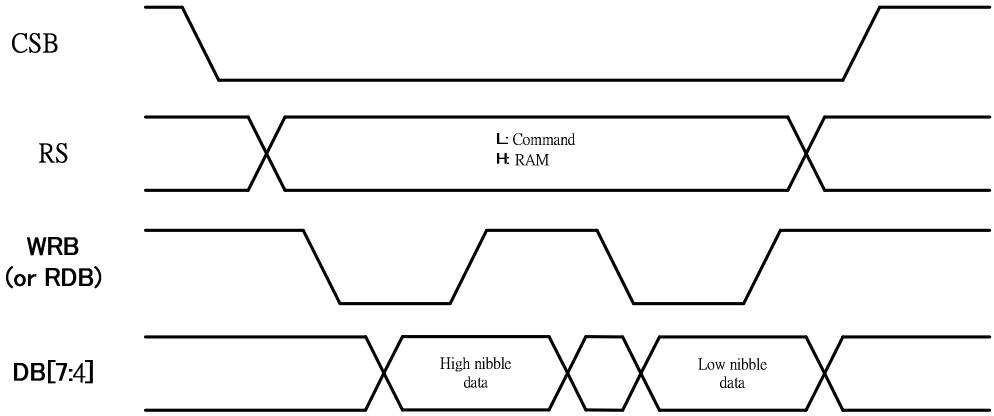
From the above timing diagram, it is important to note that the Busy Flag Check and the data transfer are both executed twice.

80 – series interface

(a) 8-BIT mode

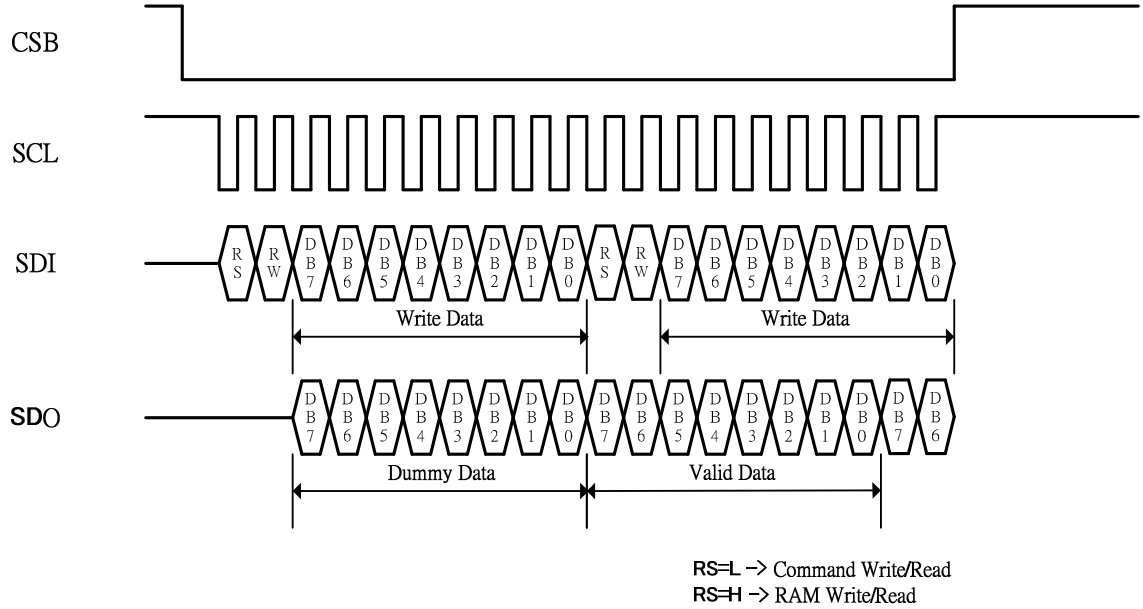


(b) 4-BIT mode



Serial interface

3-Line series Write/Read



AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

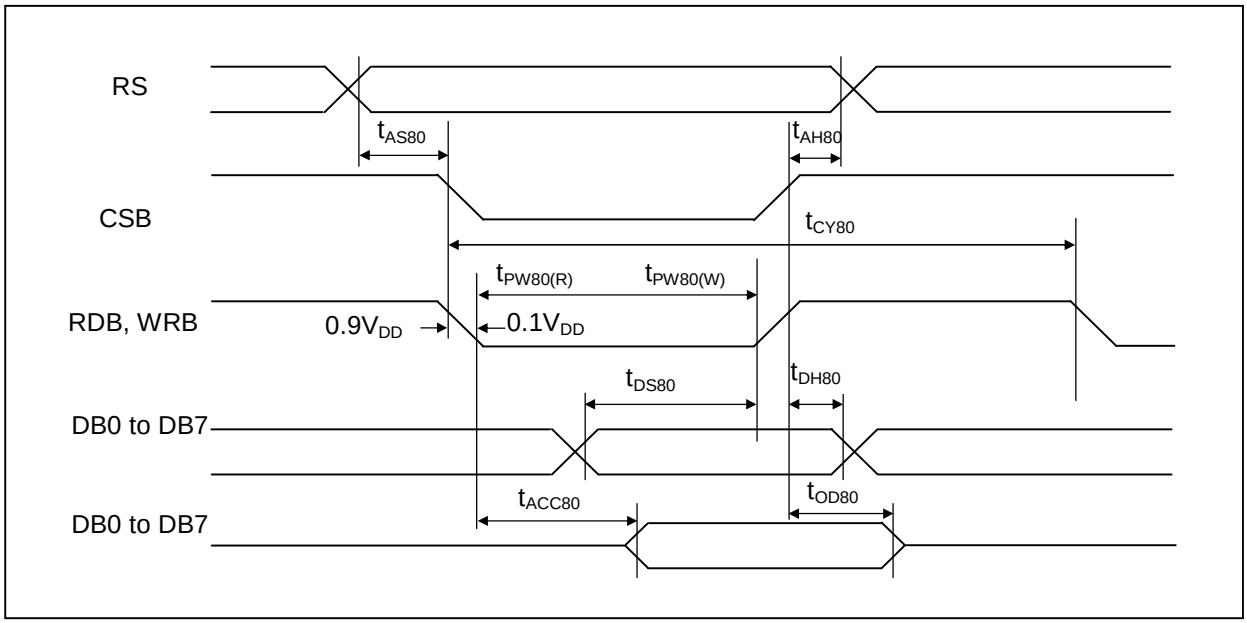


Figure 1. Read / Write Characteristics (8080-series MPU)

VDD = 3.0 to 5.3V, Ta = -40 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t**AS80** t**AH80**	0 0	-	-	ns	
System cycle time		t**CY80**	300	-	-	ns	
Pulse width (WRB)	RW_WRB	t**PW80**(W)	80	-	-	ns	
Pulse width (RDB)	E_RDB	t**PW80**(R)	80	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t**DS80** t**DH80**	40 15	-	-	ns	
Read access time Output disable time		t**ACC80** t**OD80**	- 10	-	140 100	ns	C_L = 100pF

Read / Write Characteristics (6800-series Microprocessor)

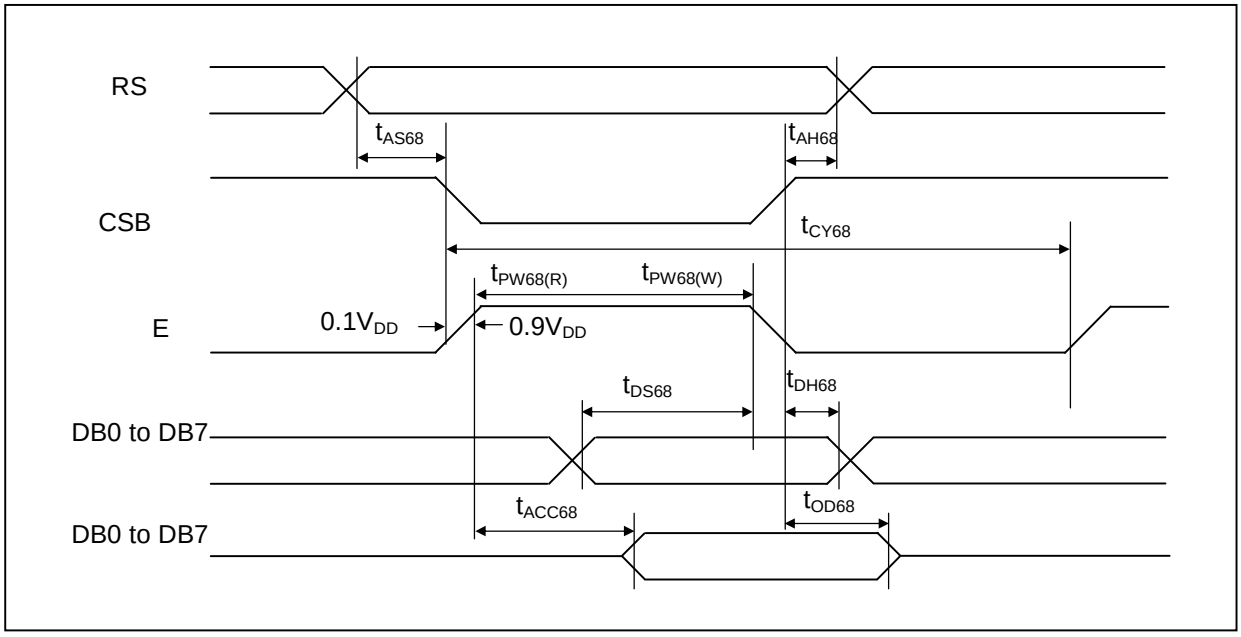


Figure 2. Read / Write Characteristics (6800-series MPU)

(VDD = 3.0 to 5.3V, Ta = -40 to +85℃)

Item	**Signal**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
Address setup time Address hold time	RS	t**AS68** t**AH68**	0 0	-	-	ns	
System cycle time		t**CY68**	300	-	-	ns	
Pulse width (E)	E_RDB	t**PW68**(W)	80	-	-	ns	
Pulse width (E)	E_RDB	t**PW68**(R)	80	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t**DS68** t**DH68**	40 0	-	-	ns	
Read access time Output disable time		t**ACC68** t**OD68**	- 5	-	70 50	ns	C**L** = 100pF

Serial Interface Characteristics

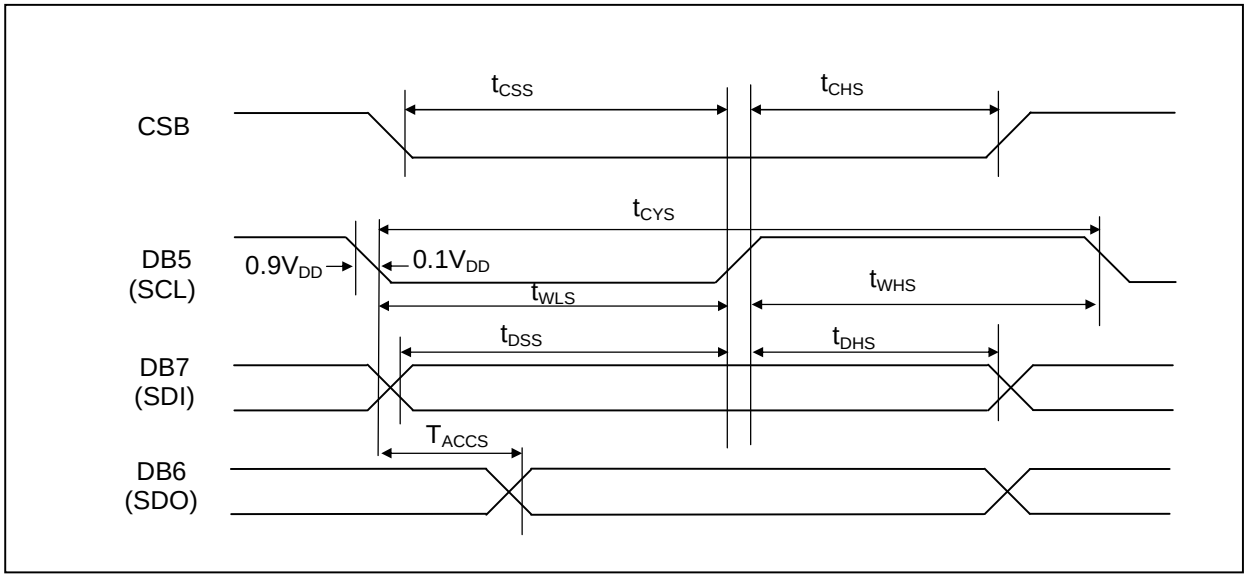


Figure 3. Serial Interface Characteristics

(VDD = 3.0 to 5.3V, Ta = -40 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB5 (SCL)	t_{CYS} t_{WHS} t_{WLS}	250 100 100	- - -	- - -	ns	
CS1B setup time CS1B hold time	CSB	t_{CSS} t_{CHS}	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	t_{DSS} t_{DHS}	100 100	- -	- -	ns	
Read access time	DB6 (SDO)	t_{ACCS}	-	-	50	ns	

13. OLED Lifetime

ITEM	Conditions	Typ	Remark
Operating Life Time	Ta=25℃ /Initial 50% check board brightness 125nits	100,000 Hrs	Note

Notes:
1. Simulation pattern for operation test: interchanging with 50% checkboard
   The brightness decay does not exceed 50%.
2. You can use the display off mode to make long life.
3. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

14. Reliability

Content of Reliability Test

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Applicable Standard**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 240hrs	——
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	80℃ 240hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40℃ 240hrs	——
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60℃,90%RH 240hrs	——
Temperature Cycle	Endurance test applying the low and high temperature cycle. -40℃ 25℃ 80℃ 30min 5min 30min 1 cycle	-40℃/80℃ 100 cycles	——
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	——
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	——
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	——
Others			
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25℃

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability. After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5℃; 55±15% RH.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for High Temperature storage, High Temperature/ Humidity Storage, Temperature Cycle

Evaluation criteria

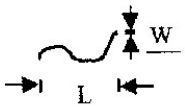
1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

APPENDIX:

RESIDUE IMAGE

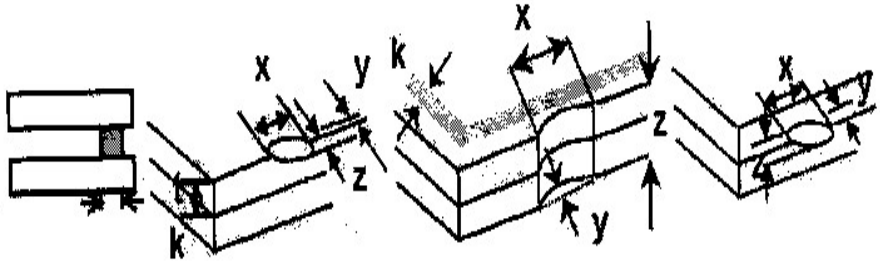
Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

15. Inspection specification

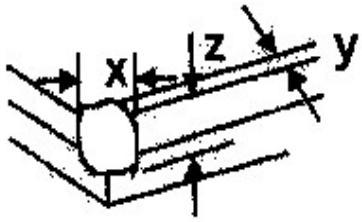
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 OLED viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on OLED (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm.</td><td>2.5</td></tr>
<tr><td>03</td><td>OLED black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2</td><td>2.5</td></tr>
<tr><td></td><td></td><td>3.2 Line type : (As following drawing)
 

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size Φ</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

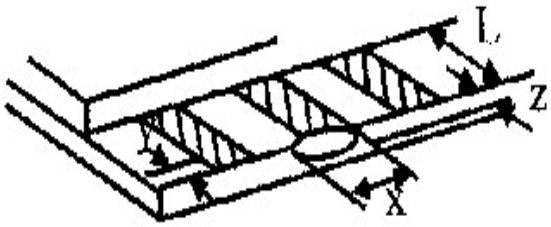
<table>
<tr><td>NO</td><td>Item</td><td>Criterion</td><td>AQL</td></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 OLED black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: OLED side length
L: Electrode pad length:

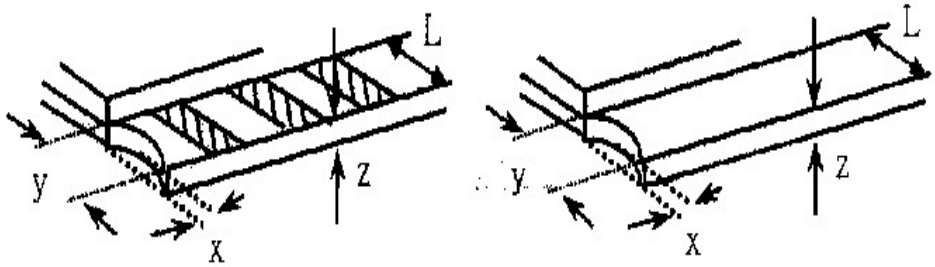
6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:
 

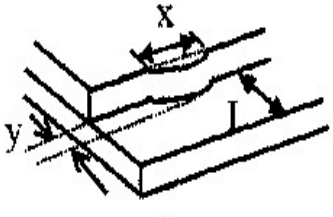
<table><tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is total length of each chip.

6.1.2 Corner crack:
 

<table><tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is the total length of each chip.</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: OLED side length
L: Electrode pad length
6.2 Protrusion over terminal :
6.2.1 Chip on electrode pad :


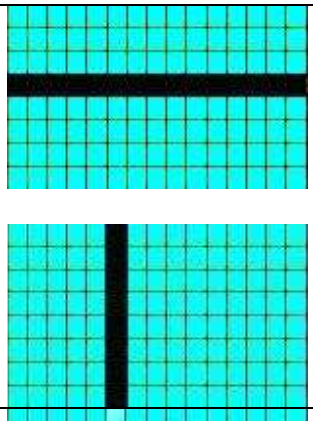
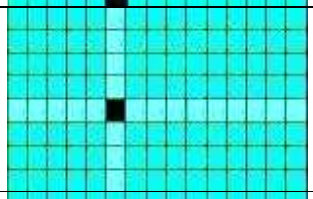
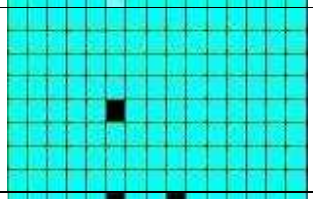
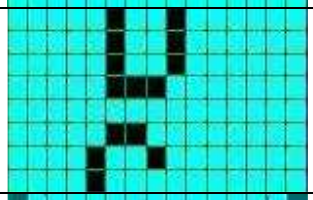
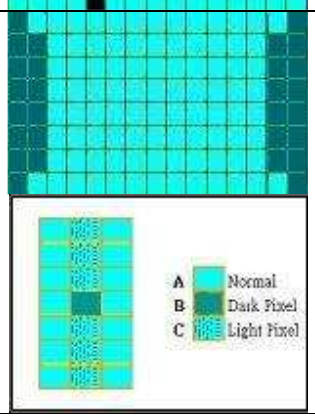
<table>
<tr><td>y: Chip width</td><td>x: Chip length</td><td>z: Chip thickness</td></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:


<table>
<tr><td>y: Chip width</td><td>x: Chip length</td><td>z: Chip thickness</td></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.
6.2.3 Substrate protuberance and internal crack.


<table>
<tr><td>y: width</td><td>x: length</td></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
07	Cracked glass	The OLCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using OLED spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, OLED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 OLED pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Short	Major	
Wrong Display	Major	
Un-uniform B/A x 100% < 70% A/C x 100% < 70%	Major	

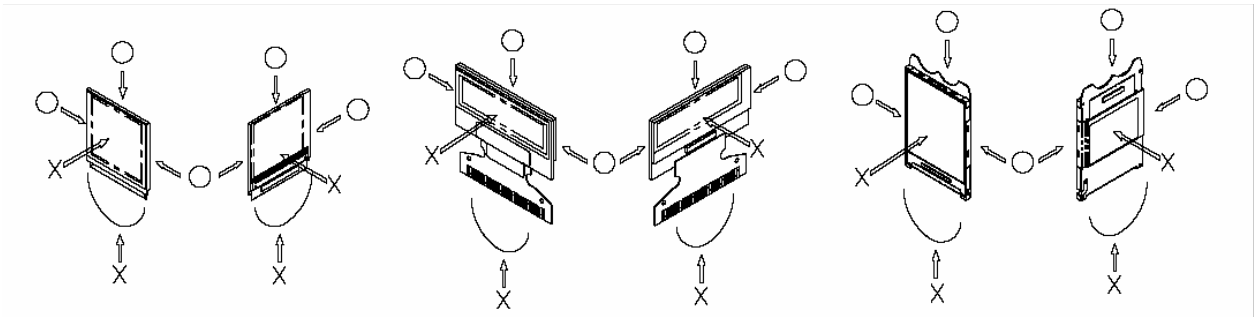
16. Precautions in use of OLED Modules-1

Modules

(1)Avoid applying excessive shocks to module or making any alterations or modifications to it.
(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED module.
(3)Don't disassemble the OLEDM.
(4)Don't operate it above the absolute maximum rating.
(5)Don't drop, bend or twist OLEDM.
(6)Soldering: only to the I/O terminals.
(7)Storage: please storage in anti-static electricity container and clean environment.

17.1 Handling Precautions

(1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
(2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
(3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
(4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
(5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
* Scotch Mending Tape No. 810 or an equivalent
Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
Also, pay attention that the following liquid and solvent may spoil the polarizer:
* Water
* Ketone
* Aromatic Solvents
(6) Hold OLED display module very carefully when placing OLED display module into the System housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts.
These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



(7) Do not apply stress to the LSI chips and the surrounding molded sections.
(8) Do not disassemble nor modify the OLED display module.
(9) Do not apply input signals while the logic power is off.
(10) Pay sufficient attention to the working environments when handing OLED display modules to prevent occurrence of element breakage accidents by static electricity.
* Be sure to make human body grounding when handling OLED display modules.
* Be sure to ground tools to use or assembly such as soldering irons.
* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
* Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.
(11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5.
(12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

(1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0℃) environments.
(We recommend you to store these modules in the packaged state when they were shipped from Winstar Technology Inc.
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
(2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

(1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
(2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
(3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
(4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
(5) As for EMI, take necessary measures on the equipment side basically.
(6) When fastening the OLED display module, fasten the external plastic housing section.
(7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

* Connection (contact) to any other potential than the above may lead to rupture of the IC.

Precautions in use of OLED Modules-2

(1)Avoid applying excessive shocks to module or making any alterations or modifications to it.
(2)Don’t make extra holes on the printed circuit board, modify its shape or change the components of OLED module.
(3)Don’t disassemble the OLEDM.
(4)Don’t operate it above the absolute maximum rating.
(5)Don’t drop, bend or twist OLEDM.
(6)Soldering: only to the I/O terminals.
(7)Storage: please storage in anti-static electricity container and clean environment.

8.4 Precautions when disposing of the OLED display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

(1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

(2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.

* Pins and electrodes
* Pattern layouts such as the TCP & FPC

(3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.

* Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
* Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.

(4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

(5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

(6)Resistors,capacitors and other passive components will have different appearance and color caused by the different supplier.

(7)Our company will has the right to upgrade and modify the product function.